Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Amended) An integrated circuit package comprising:

a silicon die having a first thickness;

a metallized polymer layer having a first side and a second side; ~~and~~

a transition medium disposed between the silicon die and the first side of the metallized polymer layer; and

a plastic encapsulant which encapsulates the silicon die and the transition medium, the plastic encapsulant and transition medium each having a coefficient of thermal expansion between approximately 7×10^{-6}/°C and 15×10^{-6}/°C,

wherein the transition medium has a second thickness,

the first thickness of the silicon die is less than the second thickness,

a first edge of the transition medium is coincident with a first edge of the silicon die, and

a second edge of the transition medium is coincident with a second edge of the silicon die.

2. (Original) The integrated circuit package of claim 1 wherein the transition medium is nonconductive.

3. (Cancelled)

4. (Previously Amended) The integrated circuit package of claim 1 wherein the transition medium comprises a mold compound material.

5. (Cancelled)

6. (Original) The integrated circuit package of claim 1 wherein the presence of the transition medium reduces stress and fracture damage to the silicon die.

7. (Previously Amended) The integrated circuit package of claim 1 wherein a thickness of the metallized polymer layer and a thickness of the plastic encapsulant define a package thickness, wherein the silicon die is disposed at a location approximately equally spaced from the bottom of the metallized polymer layer and the top of the plastic encapsulant.

8. (Original) The integrated circuit package of claim 7 wherein the package thickness is approximately 0.060 inches or less.

9. (Previously Amended) The integrated circuit package of claim 1 wherein the first thickness is less than approximately 6 mils.

10. (Original) The integrated circuit package of claim 1 wherein the silicon die is coupled to the transition medium through an adhesive.

11. (Previously Presented) The integrated circuit package of claim 10 wherein a coefficient of thermal expansion for the adhesive is approximately 58 x 10^{-6}/°C.

12. (Previously Presented) The integrated circuit package of claim 1 wherein the metallized polymer layer is a tape carrier having a dielectric layer and a conductive layer.

13. (Original) The integrated circuit package of claim 12 comprising solder balls mounted to the second side of the metallized polymer layer, the solder balls electrically contacting an etched circuit in a conductive layer of the tape carrier.

14. (Original) The integrated circuit package of claim 13 wherein the solder balls electrically connect the integrated circuit package to a printed circuit board.

15. (Original) The integrated circuit package of claim 14 wherein the solder balls are arranged in a grid fashion underneath the position for the silicon die.

16. (Original) The integrated circuit package of claim 1 wherein the cross sectional area of the silicon die is substantially less than or equal to the cross sectional area of the rigid transition medium.

17. (Previously Presented) The integrated circuit package of claim 14 wherein the silicon die has been lapped to the first thickness.

18. (Original) The integrated circuit package of claim 1 wherein the package is a BGA package.

19. (Original) The integrated circuit package of claim 1 wherein a volume of the silicon die is less than the volume of the rigid transition medium.

20. (Previously Presented) An integrated circuit package comprising:

a metallized polymer layer defining a first thickness;

at least one solder ball, the at least one solder ball and metallized polymer layer comprise a flat surface;

a transition medium coupled to the metallized polymer layer;

a die coupled to the transition medium; and

a mold cap encapsulating the transition medium and the die, the mold cap defining a second thickness,

wherein the first thickness and second thickness define a package thickness,

the transition medium and the mold cap each comprising a first mold compound, and

the die is disposed near a midline of the package thickness measured from the bottom of the metallized polymer layer to the top of the mold cap.

21. (Original) The integrated circuit package of claim 20 wherein the mold cap has a coefficient of thermal expansion similar to a coefficient of thermal expansion of the transition medium.

22. (Original) The integrated circuit package of claim 20 wherein the die is mounted to the transition medium with a layer of adhesive.

23. (Previously Presented) The integrated circuit package of claim 20 wherein a first edge of the transition medium is coincident with a first edge of the die, a second edge of the transition medium is coincident with a second edge of the die.

24. (Original) The integrated circuit package of claim 20 wherein the metallized polymer layer is a tape carrier.

25. (Previously Presented) An integrated circuit package comprising:

a tape carrier defining a thickness;

a first adhesive layer disposed on the tape carrier, the first adhesive layer having a coefficient of thermal expansion and a thickness;

a transition medium having a first surface and a second surface, wherein the first surface of the transition medium engages the first adhesive layer, the transition medium having a coefficient of thermal expansion and a thickness;

a second adhesive layer disposed on the second surface of the transition medium, the second layer of adhesive having a coefficient of thermal expansion and a thickness;

a die disposed on the second adhesive layer comprising a thickness that is less than the thickness of the transition medium, wherein a first edge of the transition medium is coincident with a first edge of the die, and a second edge of the transition medium is coincident with a second edge of the die; and

a mold cap encapsulating the first adhesive layer, the transition medium, the second adhesive layer and the die, wherein the transition medium and the mold cap each comprising a first mold compound, thereby the transition medium and the mold cap have approximately the same coefficient of thermal expansion so as to reduce the thermal stress on the die during thermal cycling.

26-48. (Cancelled)

49. (Previously Presented) An integrated circuit package comprising:

an integrated circuit die having a front side, a back side, and a first thickness between the front and back sides, wherein bonding pads are formed on the front side;

a metallized polymer layer having a first side and a second side, wherein the bonding pads are electrically coupled to features of the metallized polymer layer; and

a transition medium comprising a mold compound, between the integrated circuit die and the metallized polymer layer, wherein the transition medium has a second thickness, greater than the first thickness, a first edge of the transition medium is coincident with a first edge of the integrated circuit die, and a second edge of the transition medium is coincident with a second edge of the integrated circuit die.

50. (Previously Presented) The integrated circuit package of claim 49 wherein the front side of the integrated circuit die faces away from the metallized polymer layer.

51. (Previously Presented) The integrated circuit package of claim 49 wherein the integrated circuit die, metallized polymer layer, and transition medium are three parallel planes.

52. (Previously Presented) The integrated circuit package of claim 49 wherein the transition medium has a single, relatively uniform thickness.

53. (Previously Presented) The integrated circuit package of claim 49 wherein the integrated circuit package accommodates only a single integrated circuit die.

54. (Previously Presented) The integrated circuit package of claim 49 further comprising:

bonding wires to electrically couple the bonding pads to the features of the metallized polymer layer.

55. (Previously Presented) The integrated circuit package of claim 49 wherein the transition medium does not comprise metal.

56. (Previously Presented) The integrated circuit package of claim 49 wherein none of the bonding pads are electrically coupled to the transition medium.

57. (Previously Presented) The integrated circuit package of claim 49 wherein between the transition medium and the integrated circuit die is only an adhesive layer.

58. (Previously Presented) The integrated circuit package of claim 49 wherein the back side of the integrated circuit die faces toward the transition medium.

59. (Previously Presented) The integrated circuit package of claim 49 wherein the integrated circuit package is a ball grid array package.

60. (Previously Presented) The integrated circuit package of claim 49 wherein the transition medium has a coefficient of thermal expansion between approximately 7 x 10^{-6}/°C and 17 x 10^{-6}/°C.

61. (Previously Presented) The integrated circuit package of claim 49 further comprising:

solder balls, below the metallized polymer layer and integrated circuit die, electrically coupled to the bonding pads.

62. (Previously Presented) An integrated circuit package comprising:

a substrate;

a silicon die comprising a thickness;

a transition medium positioned between the substrate and the silicon die; and

a plastic encapsulant which encapsulates the silicon die and the transition medium,

wherein the transition medium comprises a thickness that is greater than the thickness of the silicon die, the transition medium and the plastic encapsulant each comprising a first mold compound, thereby the coefficient of thermal expansion of the transition medium is approximately equal to that of the plastic encapsulant.

63. (Previously Presented) The integrated circuit package of claim 62 wherein a first edge of the transition medium is coincident with a first edge of the silicon die, and a second edge of the transition medium is coincident with a second edge of the silicon die.

64. (Previously Presented) The integrated circuit package of claim 62 wherein the distance from the top of the plastic encapsulant to the bottom of the substrate defines a package thickness and the silicon die is positioned at approximately a midpoint of the package thickness.

65. (Cancelled)

66. (Previously Presented) The integrated circuit package of claim 62 wherein the transition medium has a coefficient of thermal expansion between approximately 7 x 10^{-6}/°C and 17 x 10^{-6}/°C.

67. (Previously Presented) An integrated circuit package comprising:

a silicon die having a first thickness;

a metallized polymer layer having a first side and a second side;

a transition medium disposed between the silicon die and the first side of the metallized polymer layer; and

a plastic encapsulant which encapsulates the silicon die and the transition medium, wherein the transition medium has a second thickness, the first thickness is less than the second thickness, the plastic encapsulant and the transition medium each comprising a first mold compound, thereby the coefficient of thermal expansion of the transition medium is approximately equal to that of the plastic encapsulant.

68. (Previously Presented) The integrated circuit package of claim 67 wherein the coefficient of thermal expansion of the transition medium is greater than the coefficient of thermal expansion of the silicon die.

69. (Previously Presented) An integrated circuit package capable of being coupled to a printed circuit board comprising:

a silicon die having a first thickness;

a metallized polymer layer;

a transition medium having a second thickness; and

a plastic encapsulant which encapsulates the silicon die and the transition medium; and

wherein the transition medium is disposed between the silicon die and the metallized polymer layer,

wherein the first thickness is less than the second thickness,

wherein a first edge of the transition medium is coincident with a first edge of the silicon die,

wherein a second edge of the transition medium is coincident with a second edge of the silicon die, and

wherein both the transition medium and the plastic encapsulant have a coefficient of thermal expansion less than the coefficient of thermal expansion of the printed circuit board to which the integrated circuit package is capable of being coupled and greater than the coefficient of thermal expansion of the silicon die.

70. (previously presented) The integrated circuit package of claim 3 wherein the coefficient of thermal expansion of the transition medium is approximately equal to that of the plastic encapsulant.